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and for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., and AEROFLEX COLORADO SPRINGS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC. Defendants.	Case No. C03-04669 MJJ (EMC) Case No. C03-02289 MJJ (EMC) **DECLARATION OF ALBERT E. CASAVANT IN SUPPORT OF SYNOPSYS AND THE CUSTOMER DEFENDANTS' MOTIONS FOR SUMMARY JUDGMENT** **FILED UNDER SEAL**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant.	

I, ALBERT E. CASAVANT, declare as follows:

1. I am an Assistant Professor in the Math and Computer Science Department at the University of Maryland Eastern Shore. I teach undergraduate and graduate Computer Science Courses. Until 2003, I was employed in industry as a researcher in the area of Electronic CAD tool design. My master's and doctoral theses were both in this area, and all of my industrial experience since 1982 has been in this area. I have created several Electronic CAD tools.

2. Attached as Exhibit 1 to this declaration is a true copy of Exhibit 1 from my Expert Report.

3. I have been retained on behalf of Aeroflex Incorporated, Aeroflex Colorado Springs, Inc., AMI Semiconductor, Inc., Matrox Electronics Systems, Ltd., Matrox Graphics, Inc., Matrox International Corp., and Matrox Tech, Inc. ("the Customer Defendants") to address infringement-related issues concerning U.S. Patent No. 4,922,432 ("the '432 patent") entitled "Knowledge Based Method and Apparatus for Designing Integrated Circuits Using Functional Specifications."

4. On July 24, 2006, I submitted a report containing my opinions on infringement-related issues concerning the '432 patent. I addressed in my report various allegations made by Ricoh Company, Ltd. ("Ricoh") that the Customer Defendants infringe claims 13-17 of the '432 patent by using Synopsys' Design Compiler system to design ASICs and came to the conclusions set forth below.

5. In forming my opinions, I have relied on my knowledge and experience in Computer Science, Electronic Design, CAD Tool Design, and Electrical Engineering. I have also considered the following information: the /vobs source code and running binary code of the V-2003.12-SP1 version of Synopsys' Design Compiler system; the '432 patent, its patent history and documents referred to in that patent; U.S. Patent number 4,703,435 ("the '435 patent") and documents referred to in that patent; Ricoh's March 23, 2006 Final Infringement Contentions and Ricoh's June 23, 2006 Supplemental Final Infringement Contentions, as well as the accompanying exhibits and documents, source code, and deposition testimony cited therein; the Court's April 7, 2005 Claim Construction Order; Ricoh's Expert Report of Marios Papaefthymiou on Infringement by Aeroflex, by AMI Semiconductor, Inc., and by Matrox and the attached exhibits; Ricoh's Written Report of Donald Soderman on Infringement by Aeroflex, by AMI, and by Matrox and the attached exhibits; the Expert Report on Validity of Patent

4,922,432 by Tom M. Mitchell; deposition transcripts of David Tran, Robert Walker, Vasant Ramabadran, Peter Milliken, Eric Boisvert, Brandon Coco, Robert B. Smith, Theodore Kowalski, David Kerwin, Reed Packer, and David Chiappini; and various other documents produced in this litigation, including Synopsys product manuals and documentation. In addition, I considered information obtained through discussions with David Tran, Robert Walker, Kristen McNall, Sharlene Gee, and David Chiappini. I have also reviewed two patents issued to Dr. Soderman: U.S. Patent Nos. 6,226,776 and 6,848,085 ("the Soderman patents"), three articles co-authored by Dr. Soderman and published in 1998 ("the Soderman articles"), and portions of the book "Introduction to HDL-Based Design Using VHDL" by Steve Carlson of Synopsys, Inc., published in 1991.

6. I understand from counsel for Synopsys and the Customer Defendants that Ricoh's infringement claim is known as a literal infringement claim. It is my further understanding that the test for literal infringement is as follows: to decide whether an alleged infringer's method literally infringes a claim of a patent, you must compare that method with the patent claim and determine whether every requirement of the claim is included in that method. If so, the alleged infringer's method literally infringes that claim. If, however, the alleged infringer's method does not have every requirement in the patent claim, the alleged infringer's method does not literally infringe that claim. I have applied this understanding of the law on literal infringement in my analysis of Ricoh's infringement allegations.

7. Claim 13 of the '432 patent reads:

> A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising:
>
> [A] storing a set of definitions of architecture independent actions and conditions;
>
> [B] storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;
>
> [C] storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;
>
> [D] describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;
>
> [E] specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and

> [F] selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

I have labeled each element of this claim with the letters A-F for easy reference.

Claim 13, Preamble

8. The preamble of claim 13 provides that the claimed method is a "computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising . . . ." It is my opinion that the Customer Defendants do not meet the requirements of the preamble because many of the accused ASICs were not designed, in their entirety, using Design Compiler. First, Aeroflex, Matrox, and AMI all use Design Compiler to design only the digital portion of what are known as mixed signal ASICs. Mixed signal ASICs are ASICs that have an analog and a digital portion. In the case of the accused Aeroflex, Matrox, and AMI accused products a large number of the accused ASICs are mixed signal ASICs for which the analog portion of the designs was not designed using Design Compiler. Attached hereto as Exhibit 2 is a list of the accused products I understand to be mixed-signal products.

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10. Moreover, there are other portions of an ASIC that Design Compiler does not synthesize. For example, Design Compiler does not synthesize instantiating pad cells, asynchronous logic, and hand-instantiated logic.

Claim 13, Element A

11. Element A of '432 Claim 13 reads: "storing a set of definitions of architecture independent actions and conditions." The Court construed "a set of definitions of architecture independent actions and

conditions" as "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC." The Court did not construe the meaning of the word "definitions" in this element. Thus, I have looked to the specification of the patent for guidance as to what was intended by the inventors. Based on my review of the specification, the definitions appear to have been the macros described in the patent. There is little specificity about what the macros actually are in the context of the patent (largely explained by the fact that the specification talks only about flowchart input). This is the only passage in the patent that describes the macro library (i.e., the set for stored definitions):

> with a given type. The macro library 23 contains a set of macros defining various actions which can be specified in the flowchart. For each macro function in the macro library 23 there may be several hardware cells in the cell library 34 of differing geometry and characteristics capable of performing the specified function. Using a

12. The patent also contains the following passage regarding use of the macros in the cell selection process:

> In the cell selection process, the above information can be used. Some parameters that can be used to map macros to cells are:
> (1) name of macro
> (2) function to be performed
> (3) complexity of the chip
> (4) fabrication technology
> (5) delay time allowed
> (6) power consumption
> (7) bit size of macro data paths

This list would suggest that at least these some of these attributes must be contained in the "definition" of the actions and conditions.

13. The specification also says the following with regard to the use of the macro definitions:

> lected by PSCS. PSCS also uses the macro definitions for connecting the cell terminals to other cells. PSCS

This would suggest that the stored definitions must include information for connecting the cell terminals to other cells. Based on this information contained in the specification, the definitions should include the

name of the macro, the function of the macro, the list of cells that can implement the macro, the bit size of the macro data path, and information needed to connect cell terminals to other cells. I understand that Dr. Soderman now claim in his deposition that the names of the generic operators alone constitute the definitions. Whether or not the Court agrees that the "definitions" must include some or all of the information above, it is my opinion that, at a minimum, the name of the operator alone cannot constitute a definition.

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21. Dr. Soderman asserts in his expert report (p. 25) that the "specifying" step (element E) occurs in HDL Compiler. Based on Ricoh's Infringement Contentions regarding the specifying step, the stored definitions must be the in the output of HDL Compiler. Another way of saying this is that the input descriptions must be mapped to the "stored definitions" during the "specifying" step.

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23. For at least the reasons set forth above, it is my opinion that what Ricoh alleges as constituting the "library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC" within the Design Compiler system does not in fact meet the requirements of element A.

Claim 13, Element B

24. Element B of claim 13 reads: "storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set." I have analyzed what I understand to be exemplary technology libraries

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It is my conclusion that these technology libraries do not meet the requirements of this claim element because the "hardware cells" that are selected from in the selecting step are not selected "from" what is contained in the technology libraries as contemplated by the claim.

25. Rather, it is my conclusion that the technology libraries at issue contain simple logic gates. Indeed, what is contained in the technology library are basic logic gates, not technology specific implementations of hardware cells that correspond to the architecture independent actions and conditions. Instead, the library is comprised of a variety of AND, OR, XOR, and other simple logic gates. In addition, there is no geometrical data regarding the mask level specification of any hardware cells in the technology libraries. If an 8 bit ripple carry adder is requested, only a one bit of that adder is stored in the technology

library. Design Compiler must then "assemble" the bit slices to produce the full operator as described in the HDL input.

26. Thus, Design Compiler is not storing a "set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set" as claimed, because Design Compiler cannot possibly select from the "cells" stored in the technology libraries to implement the alleged definitions of actions and conditions.

27. Moreover, this library does not meet the requirement that the hardware cells that will ultimately be selected are stored in memory prior to the selecting step. To the contrary, these cells will not be selected, and thus, cannot meet this requirement.

28. Finally, these simple logic gates cannot be said to meet the limitation of the final element of "mapping the specified stored function (action and condition) to a corresponding stored hardware cell" because a +, for example, will not be mapped to the simple logic gates contained in the library.

29. Accordingly, it is my opinion that the requirements of this element are not met by the storing of the technology library as Ricoh alleges.

Claim 13, Element C

30. Element C of claim 13 reads: "storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions." This element refers to storing "rules" to select hardware cells from among those stored in element B to execute the definitions of architecture independent actions and conditions specified in element E. Specifically, the "rules" stored in this step are used in the "selecting" step of Element F. That step reads: "selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells . . . ." Accordingly, one requirement of the rules is that they must be applied to the specified definitions to select the cells in Element F.

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Claim 13, Element D

37. Element D of claim 13 reads: "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions." I understand that the court construed "architecture independent actions and conditions" as "functional or behavioral aspects of a circuit (or circuit segment) that does not imply a set architecture, structure, or implementing technology, but excludes

the use of register-transfer level descriptions as taught in Darringer." Claim Construction Order at 12:17-19.

38. I note that immediately preceding this statement, and after discussing and rejecting Ricoh's attempt to make a distinction between structural and functional RTL, the Court states "Furthermore, an examination of the patent's public record fails to provide any support for Ricoh's distinction between 'structural' and 'functional' RTL-type input systems. Given these findings, Ricoh's attempt to limit the patentee's disclaimer to only 'structural' level RTL-type input systems is unpersuasive . . . . Accordingly, the prosecution history indicates that the patentee expressly disclaimed all register transfer level descriptions." Claim Construction Order at 12:9-15.

39. Despite this statement that "all register transfer level descriptions" were expressly disclaimed by the '432 patentee, for purposes of my analysis I have applied the Court's construction of "architecture independent actions and conditions" as "functional or behavioral aspects of a circuit (or circuit segment) that does not imply a set architecture, structure, or implementing technology, but excludes the use of register-transfer level descriptions as taught in Darringer."

40. It is my opinion that the Defendants in this case use register-transfer-level (RTL) inputs as defined in Darringer. The Darringer patent referenced by the Court in its claim construction order defines register-transfer-level inputs. Specifically, the Darringer patent defines RTL descriptions as descriptions that consist of two parts: "a specification of the inputs, outputs and latches of the chip to be synthesized; and a flowchart-like specification of control, describing for a single clock cycle of the machine how the chip outputs and latches are set according to the values of the chip inputs and previous values of the latches." The Court referenced this definition in reaching its conclusion that architecture independent actions and conditions exclude register-transfer-level descriptions as taught in Darringer.

41. My review of exemplary Defendant inputs confirms that they are Darringer RTL. The Defendants' input descriptions specify the inputs, outputs, and latches of the chip to be synthesized. The Defendants' input descriptions also contain a specification of control describing for a single clock cycle of the machine how the chip outputs and latches are set according to the values of the chip inputs and previous

values of the latches. Thus, it is my opinion that the Defendant inputs do not meet the requirements of this element.

42. Regardless of whether this description of the inputs, i.e., that the input descriptions specify the inputs, outputs, and latches of the chip to be synthesized and also contain a specification of control describing for a single clock cycle of the machine how the chip outputs and latches are set according to the values of the chip inputs and previous values of the latches, is "RTL" or not, it describes, in my opinion, input that is not architecture independent. In my view, if an input description meets this definition, regardless of whether it includes HDL operators to describe input functions, it is a functional or behavioral description of aspects of a portion of a circuit (or circuit segment) that does imply a set architecture.

43. Moreover, it is my opinion that Design Compiler is not capable of performing synthesis of non-netlist VHDL or Verilog inputs unless the inputs meet the above Darringer RTL/not architecture independent definition.

44. Design Compiler requires the type of input defined by Darringer to create the design for a working ASIC. If any element of the above description as it applies to the hardware being designed is removed from input to Design Compiler, then Design Compiler would not be able to create a working ASIC design. The description of what needs to be designed must include all of the elements of Darringer's definition to be a legal input to Design Compiler (in all but the most trivial designs). Thus, Design Compiler's required input description encompasses Darringer's description of RTL. If the Defendants did not use RTL to describe their designs, then Design Compiler could not help them design their ASICs. In particular, an important necessary characteristic for obtaining meaningful results from Design Compiler is that one observes the same behavior by simulating the input RTL and the output netlist.

45. I have reviewed two patents issued to Dr. Soderman: U.S. Patent Nos. 6,226,776 and 6,848,085 ("the Soderman patents"), three articles co-authored by Dr. Soderman and published in 1998 ("the Soderman articles") (which were introduced as Exhibits 4-6 at the Soderman deposition), and portions of the book "Introduction to HDL-Based Design Using VHDL" by Steve Carlson of Synopsys, Inc., published in 1991.

46. The Soderman patents, the Soderman articles, and Mr. Carlson's book are all consistent with my opinion that Design Compiler requires the user to input an RTL description that meets the Darringer definition of RTL to create a design for a working ASIC and is not architecture independent.

47. I have also reviewed the August 14, 2006 deposition transcript of Dr. Soderman, and Dr. Soderman's testimony is also consistent with my opinion. A true and correct copy of excerpts from Dr. Soderman's August 14 deposition transcript is attached hereto as Exhibit 3 [8/14 Soderman Depo. Tr. 49-56, 77-80, 108]. In the excerpts, Dr. Soderman agrees that in 1997, users of synthesis tools such as Synopsys' Design Compiler system needed to input into those tools RTL descriptions having the same characteristics as RTL defined in Darringer. Dr. Soderman also agrees that the accused Customer Defendant designs have the same characteristics as the RTL defined in Darringer.

48. Mr. Carlson's book perhaps states this point most concisely. Mr. Carlson states, in the context of describing the input to Synopsys' Design Compiler system, that "The input to HDL synthesis is an RTL (register transfer level) functional description of the network to be implemented. RTL descriptions are distinct from behavioral level descriptions. The distinction is that a behavioral description has no implied architecture in its representation, while an RTL level description has a definite, implied architecture." (p. 3). Thus, the input into the Design Compiler system – regardless of what one chooses to call it – must have a defined architecture that is set before it is input into the system, and therefore cannot be a description of "architecture independent actions and conditions."

Claim 13, Element E

49. Element E of claim 13 reads: "specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed." The Court construed "specifying for each described action and condition of the series one of said stored definitions" as "specifying for each desired functional specification to be performed by the desired ASIC one of the definitions from the set of stored definitions." Claim Construction Order at 22. Thus, element E describes a "mating up" of actions and conditions described in element D with the definitions of actions and conditions stored in element A.

50. Based on the language of the Court's claim construction that "one of the definitions" from the stored set must be specified "for each desired functional specification to be performed," element E requires that every desired function described in element D must be mated up with a corresponding definition that was stored in element A. This element therefore requires that there be one stored action or condition for each described action or condition.

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It is therefore my opinion that one would need to analyze each design on a design by design basis to determine whether such a one-to-one correspondence exists.

Claim 13, Element F

52. Element F requires the step of "selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell." The Court construed this phrase as "mapping the specified stored function to a corresponding stored hardware cell." Claim Construction Order at 20. The "specified stored function" here refers to the Element A definitions that were specified in Element E, while the "corresponding stored hardware cells" refers to the hardware cells that were stored in Element B. Thus, Element F involves the "mating up" of definitions from Element A (as specified in Element E) with hardware cells stored in Element B.

53. The language of Element F refers to "selecting from said stored data for ***each*** of the specified definitions ***a*** corresponding integrated circuit hardware cell." Emphasis mine. This language indicates that there must be a one-to-one correspondence between each specified definition and a corresponding hardware cell. Because there must be a one-to-one correspondence between the described actions and conditions and the specified definitions and then there must be a one-to-one correspondence between the specified definitions and the hardware cells, there must be a one-to-one correspondence between the described actions and conditions and the selected hardware cells.

54. With regard to the one-to-one correspondence between the specified definitions and/or the one-to-one correspondence between described actions and conditions and the selected hardware cells, there

are many circumstances in which there would be no one-to-one correspondence. It is therefore my opinion that one would need to analyze each design on a design by design basis to determine whether such a one-to-one correspondence exists.

Claim 14

55. Claim 14 reads: "A process as defined in claim 13, including generating from the netlist the mask data required to produce an integrated circuit having the desired function." Claim 14 extends claim 13 by adding a step of generating mask data for the netlist generated in claim 13, element F.

56. In my previous analysis of claim 13, it was my opinion that the defendants in this case did not infringe upon the '432 patent. Since claim 14 includes the claim 13 process, the defendants have not, in my opinion, infringed on claim 14. In addition, it is my opinion that the netlist generated by the ASIC Designer using Design Compiler is not used in the creation of mask data for the accused ASICs, as required in claim 14.

57. In ASIC design, there historically have been two different design phases. The first, the logic design phase, is covered more or less by tools such as Design Compiler. The second phase, physical design, involves the use of completely different tools whose goal is to do the "physical design" of the ASIC, i.e., transform the netlist output by tools such as Design Compiler into one that is suitable for physical production of the ASIC. The ASIC design process resembles a "chicken and egg" problem. The logic design of an ASIC influences the physical design, because to meet time delay constraints, gates are "sized" by the logic design tools, but then those sizes may not be appropriate for physical design.

58. The basic problem is that once logic gates are placed and routed on the ASIC, the delay assumptions made by the logic synthesis tool are no longer valid. The distances between the gates on the chip (not fully predictable in the logic design phase) changes the actual delay of the circuit. At that point, the logic design must be modified and gates must be sized again to meet delay constraints. Hence, the physical design influences the logic design.

59. The back and forth "chicken and egg" problem may take several applications of logic design followed by physical design before the logic design tool has accurate enough delay estimates to do its job properly and the physical design tool does not need to modify the IC layout to meet the timing

constraints. This problem is frequently called "the timing closure problem." As IC geometries shrink, the effect of "routing delays" becomes a high fraction of total delay. Because of this, the timing closure problem has become increasingly difficult to solve.

60. Thus, it is not reasonable to expect that a netlist that is the output of Design Compiler can be used directly to produce an ASIC. Although this is possible, it is extremely unlikely, especially in high performance designs where timing closure is difficult to achieve. The netlist needs to be modified, perhaps several times. This would involve not only sizing changes, but also changes in the Boolean logic implementation. Thus, the output of Design Compiler is unlikely to be "a description of the hardware components (and their interconnections) needed to manufacture the ASIC as used by subsequent processes, i.e., mask development, foundry, etc."

Claim 16

61. Claim 15 of the '432 patent reads: "A process as defined in claim 13, including the further step of generating data paths for the selected integrated circuit hardware cells." Claim 16 reads: "A process as defined in claim 15 wherein said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom." Claim 16 extends claim 15 (and thus claim 13) to include generating the data paths of claim 15 using "data path rules."

62. In my previous analysis of claim 13, it was my opinion that the defendants in this case did not infringe upon the '432 patent. Since claim 16 includes the claim 13 process, the defendants have not, in my opinion, infringed on claim 16

gates.

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I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. This declaration was executed at Salisbury, Maryland on August 18, 2006.

By: Albert E. Casavant
Albert E. Casavant

EXHIBIT 1

Mixed-Signal and BIST-Only Products

Accused Aeroflex Mixed-Signal Products

1. JW01
2. YA04/YA13
3. YB01
4. DA01
5. DA02
6. JW02

- Source: 1/20/06 Milliken Depo. Tr. at 49, 61; 1/19/06 Kerwin Depo., Ex. 138 (8/12/05 Decl. of Brandon Coco of Aeroflex in Support of Defendants' Stipulation to Representative Products); 1/19/06 Kerwin Depo Tr. at 127-28

Accused Matrox Mixed-Signal Products

1. Cyclone (MGI)
2. Eclipse (MGI)
3. Eclipse PCI (MGI)
4. Calao (MGI)
5. Toucan (MGI)
6. Condor (MGI)
7. Condor Plus (MGI)
8. Parhelia (MGI)
9. Sundog (MGI)
10. Parhelia8x (MGI)
11. Sunex (MGI)
12. Maven (MGI)
13. Rainbow Runner (MTI)
14. Twister (MTI)

- Source: Discussion with David Chiappini

Accused AMI Mixed-Signal Products

1. 11241-801, 802, 803
2. 0QJBW-001, 002, 900, 901, 902, 903, 904, 905, 906
3. 11636-501
4. 14167-001
5. 14948-501, 502, 503
6. 15088-501
7. 15124-501, 502

8. 19007-001
9. 19075-001, 002, 003
10. 19320-001
11. 19371-001
12. 19402-001
13. 0JGBE-001, 002, 900, 901, 902
14. 19293-001, 002, 004
15. 19070-001, 002
16. 19134-001
17. 0MNTA-900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914
18. 13855-501
19. 15078-001, 002
20. 19219-001, 002, 003
21. 19299-001
22. 19409-001, 002, 003
23. 19428-001
24. 19429-001, 002, 003
25. 19529-001
26. 19558-002
27. 19608-001
28. 19645-001
29. 19664-002
30. 19693-001, 002
31. 0AFCB-002
32. D1AFCC
33. 0APSE-002
34. 0C621-003
35. 0C622-003
36. D1CORC
37. D1CORD
38. 0HISB-001
39. 0IEBA-002
40. D1SEBA

- Source: 6/1/06 Corrected Third Supplemental Product Declaration of Robert B. Smith of AMI; 3AMI 2585932-40; 6/8/06 Packer Depo. Tr. at 84-86

Accused AMI BIST-Only Products

1. 11042-002
2. 11155-001
3. 11248-001
4. 11253-001
5. 11466-501

6. 11498-502
7. 11502-001
8. 11508-001
9. 11508-002
10. 11556-502
11. 11610-501
12. 11616-501
13. 11623-001
14. 11644-001
15. 11650-501
16. 11651-501
17. 11651-502
18. 11652-501
19. 11664-501
20. 11677-501
21. 11688-501
22. 11688-502
23. 11698-501
24. 11700-501
25. 11722-501
26. 11765-001
27. 11767-501
28. 11769-501
29. 11775-501
30. 11810-501
31. 11821-501
32. 11851-001
33. 11854-501
34. 11871-501
35. 11894-501
36. 11918-001
37. 11925-501
38. 11931-502
39. 11933-501
40. 11949-501
41. 11966-501
42. 11981-001
43. 11983-501
44. 11983-502
45. 11984-501
46. 11989-501
47. 11998-501
48. 12001-501
49. 12032-501
50. 12040-501
51. 12041-001

52. 12043-501
53. 12071-001
54. 12105-001
55. 12117-501
56. 12135-501
57. 12163-501
58. 12178-001
59. 12184-501
60. 12198-501
61. 13520-511
62. 13612-441
63. 13612-501
64. 13619-501
65. 13648-501
66. 13658-501
67. 13658-502
68. 13704-501
69. 13722-501
70. 13740-501
71. 13747-501
72. 13747-502
73. 13747-503
74. 13747-504
75. 13747-505
76. 13747-506
77. 13747-507
78. 13757-501
79. 13757-502
80. 13757-503
81. 13775-502
82. 13775-504
83. 13780-501
84. 13782-001
85. 13796-501
86. 13796-502
87. 13796-503
88. 13829-501
89. 13844-501
90. 13969-501
91. 13970-501
92. 13972-501
93. 13990-001
94. 14050-501
95. 14095-501
96. 14097-501
97. 14101-501

98. 14125-501
99. 14126-501
100. 14132-501
101. 14132-502
102. 14132-503
103. 14132-504
104. 14132-506
105. 14134-502
106. 14152-501
107. 14152-502
108. 14164-001
109. 14164-002
110. 14172-501
111. 14172-502
112. 14172-503
113. 14215-502
114. 14219-501
115. 14219-502
116. 14242-502
117. 14246-501
118. 14259-501
119. 14280-501
120. 14280-502
121. 14289-001
122. 14296-501
123. 14911-501
124. 14918-501
125. 14970-501
126. 14975-501
127. 14996-501
128. 14999-501
129. 15000-501
130. 15025-512
131. 15068-501
132. 15081-501
133. 15085-001
134. 15127-502
135. 18018-001
136. 18018-010
137. 18021-004
138. 18021-201
139. 18021-207
140. 19003-001
141. 19006-001
142. 19026-001
143. 19026-002

144. 19128-001
145. 19170-001
146. 19176-001
147. 19199-001
148. 19224-002
149. 19275-001
150. 19301-001
151. 19324-001
152. 19337-001
153. 19337-002
154. 19337-003
155. 19361-001
156. 19374-001
157. 19384-001
158. 19385-001
159. 19405-001
160. 19457-001
161. 19512-001
162. 0ACAA-001
163. 0FLHG-900
164. 0FLHG-901
165. 0FLHG-902
166. 0FLJA-900
167. 0FLJF-900
168. 0FLJF-901
169. 0FLJF-902
170. 0RD1V-900
171. 11767-502
172. 11796-501
173. 11893-501
174. 11893-502
175. 11894-502
176. 11921-501
177. 11989-502
178. 11999-501
179. 12068-501
180. 12068-502
181. 12068-503
182. 12068-504
183. 13640-501
184. 13775-501
185. 13852-501
186. 14094-501
187. 14132-505
188. 14132-507
189. 14242-501

190. 14918-502
191. 14980-501
192. 14990-501
193. 14997-001
194. 15075-501
195. 15098-501
196. 15127-501
197. 18021-209
198. 18024-004
199. 18024-006
200. 19077-001
201. 19102-010
202. 19140-001
203. 19141-001
204. 19170-002
205. 19226-001
206. 19306-001
207. 19306-002
208. 19308-001
209. 19309-001
210. 19309-002
211. 19316-001
212. 19316-002
213. 19316-003
214. 19326-001
215. 19357-001
216. 19382-001
217. 19395-001
218. 19406-001
219. 19406-002
220. 19418-001
221. 19421-001
222. 19430-001
223. 19462-001
224. 19493-001
225. 19497-001
226. 19505-001
227. 19524-001
228. 19543-001
229. 19555-001
230. 19555-002
231. 19560-001

- Source: 6/1/06 Corrected Third Supplemental Product Declaration of Robert B. Smith of AMI, at 5-10